

IPC-2515A

Sectional Requirements for Implementation of Bare Board Product Electrical Testing Data Description [BDTST]

"The data model of this standard shall be in effect until 2001-12." At that time, the committee will consider changes, revision, other actions.

IPC-2515A

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A standard developed by IPC

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Adopted October 6. 1998

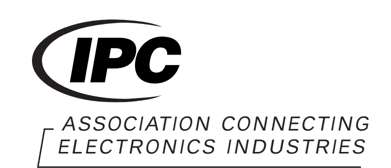
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IPC-2515A

GenCAM
[BDTST]

Sectional Requirements for Implementation of Bare Board Product Electrical Testing Data Description

A standard developed by the Computerized Data Format Standardization Subcommittee (2-11) of the Data Generation and Transfer Committee (2-10) of the Institute for Interconnecting and Packaging Electronic Circuits.

The GenCAM format is intended to provide CAD-to-CAM, or CAM-to-CAM data transfer rules and parameters related to manufacturing printed boards and printed board assemblies. The requirements of IPC-2511 are a mandatory part of this sectional standard.

This standard is part of the GenCAM 1.5 release.

"The data model of this standard shall be in effect until 2001-12." At that time, the committee will consider changes, revision, other actions.

Users of this standard are encouraged to participate in the development of future revisions.

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Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the IPC Data Generation and Transfer Committee of the IPC Data Transfer Solution DTS Subcommittee are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

Data Generation and Transfer Committee

Chairman
Harry Parkinson
Digital Equipment

Data Transfer Solution DTS Subcommittee

Chairman
Harry Parkinson
Digital Equipment

Technical Liaisons of the IPC Board of Directors

Stan Plzak
Pensar Corp.

Peter Bigelow
Beaver Brook Circuits Inc.

Special Note of Thanks

Key Individuals — An executive group of personnel from different computer disciplines helped to make this document possible. To them and their dedication, the IPC extends appreciation and gratitude. These individuals are:

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Sectional Requirements for Implementation of Bare-Board Product Testing Data Description (BDTST)

1 SCOPE

This standard specifies data formats used to describe printed board assembly in-circuit testing methodologies. These formats may be used for transmitting information between printed circuit board designers and printed board manufacturers. The formats are also useful when the manufacturing cycle includes computer-aided processes and numerical control machines.

The information can be used for both manual and for digital interpretation. The data may be defined in either English or SI units.

1.1 Interpretation

"Shall", the emphatic form of the verb, is used through this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a shall requirement is not permitted, the compliance test modules (CTMs) developed to check syntax, semantics and completeness, will prompt the user to correct the ambiguity, or to insert missing information.

1.2 Bare Board Product Testing Focus

The GenCAM format requirements are provided in a series of standards focused on printed board manufacturing, assembly, inspection, and testing. This standard, IPC-2515, provides information on bare board product testing requirements and documentation methodology. The generic standard, IPC-2511, contains general requirements and is a mandatory part of the requirements of this standard, and provides general information necessary to completely understand the GenCAM structure.

2 APPLICABLE DOCUMENTS

The following documents contain provisions which, through references in the text, constitutes provisions of IPC-2515. At the time of publication, the additions indicated were valid. All documents are subject to revision and parties to agreements based on this generic standard are encouraged to investigate the possibility of applying the most recent additions of the documents indicated below.

IPC-T-50		Terms and Definitions for Interconnecting and Packaging Electronic Circuits
IPC-2511	(MANGN)	Generic Requirements for Implementation of Product Manufacturing Description Data and Transfer
IPC-2512	(ADMIN)	Sectional Requirements for Implementation of Administrative Methods for Manufacturing Data Description
IPC-2513	(DRAWG)	Sectional Requirements for Implementation of Drawing Methods for Manufacturing Data Description
IPC-2514	(BDFAB)	Sectional Requirements for Implementation of Printed Board Fabrication Data Description.
IPC-2516	(BDASM)	Sectional Requirements for Implementation of Assembled Board Product Manufacturing Data Description
IPC-2517	(ASEMT)	Sectional Requirements for Implementation of Assembled In-Circuit Testing Data Description

IPC-2518	(PTLST)	Sectional Requirements for Implementation of Part List Product Data Description
IPC-2519	(MODEL)	Sectional Requirements for Information Model Data Related to the Printed Board and Printed Board Manufacturing Descriptions.

3 REQUIREMENTS

The requirements of IPC-2511 are a mandatory part of the standard. The IPC-2511 document describes the generic requirements of the GenCAM format. The format specifies details specifically for information interchange of data related to printed board manufacturing, assembly and test.

GenCAM is comprised of twenty sections as described in the generic GenCAM standard, IPC-2511. The sections are shown in Tables 3-1 and 3-2 of the IPC-2511.

Each section has a specific function or task respectively and is independent of each other. Accordingly, the information interchange for a specific purpose is possible only if the sections required for such a purpose have been prepared.

3.1 Categories and Content

Table 3-1 (below) provides the section names that are appropriate for the printed board assembly testing process. The letter **"M"** signifies a mandatory requirement. The letter **"O"** signifies an optional characteristic that may or may not be pertinent to the particular file. A dash signifies an extraneous section (unnecessary); CTMs will not reject file summaries if extraneous sections are present.

Table 3-1 signifies two requirement conditions separated by a "/". The first representation of requirements is intended to convey those GenCAM sections that **shall** be available as the initial input to the Bare Board test processes. The second instance of a requirement is to signify those data that **shall** be available once the processing descriptions have been completed.

Table 3-1 GenCAM Section Relationships for Bare Board Test

Section Identifiers	Bare Board Test Program Generation	Bare Board Test Fixture Generation
HEADERS	M/M	M/M
ADMINISTRATION	M/M	M/M
PRIMITIVES	M/M	M/M
ARTWORKS	M/M	M/M
LAYERS	O/O	M/M
PADSTACKS	-/-	M/M
PATTERNS	M/M	M/M
PACKAGES	-/-	-/-
FAMILIES	-/-	-/-
DEVICES	O/O	O/O
MECHANICALS	-/-	-/-
COMPONENTS	O/O	M/M
ROUTES	M/M	M/M
POWER	O/O	-/-
TESTCONNECTS	M/M	O/M
BOARDS	M/M	M/M
PANELS	O/O	O/O
FIXTURES	M/M	M/M

Section Identifiers	Bare Board Test Program Generation	Bare Board Test Fixture Generation
DRAWINGS	O/O	O/-
CHANGES	-/O*	-/O*

*The CHANGES section is used independently to alter previously sent files. Included **shall** be a HEADER section (for revision status and identification) and an ADMINISTRATION section to show effectivity

3.1.1 Bare Board Test

This document enumerates and explain the data requirements of the bare board, test step of the electronic circuit board manufacturing process. Data needs are described in the context in which they are used, and where assumptions are made, an attempt has been made to explain them. The overall effort is meant to identify and categorize data, to a reasonably, but vendor independent level. Not all data will be applicable to all situations, but any data that may be required should be listed and be provided with a syntax and location within the standard's data sets.

3.1.2 Fundamental Assumptions

This specification considers those parameters for visual inspection and electrical testing of the board. Physical metrics of material presence and thickness are supported, other process quality parameters (e.g. solderability, salts contamination) are included through references to the appropriate standard. Visual, guided visual and automated optical inspection are understood to be non-electrical test methods that are typically applied to board layers at intermediate steps of the process. Electrical bare board test is understood to be the measurement and comparison of an expected response to a recorded response, having properties of conductance, resistance, capacitance and impedance. Electrical tests are typically go, no-go tests on the completed board.

- **Opens/Shorts Test -** This is a series of resistance measurements taken end-to-end on each trace segment to assure the continuity of the conductor, and its isolation from all other traces.
- **Embedded (Printed) Component Test –** These are more sophisticated measurements, rivaling those of assembled board in-circuit test. These tests require more information pertaining to the component data, including expected nominal values and tolerances.
- **Time Domain Reflectometry (Impedance) Test** – This test is executed when specific trace impedance or impedance matching between traces is specified. The test involves the injection of a voltage pulse and measurement of its echo.
- **High-Potential Test -** As the name implies, these tests involve low current, but very high voltage measurements which further assure the isolation between traces.

3.1.3 Assembly Identification Requirements

The first of the identification requirements is the overall assembly identifier for the coupon, board, or panel. This is typically an internal part number, product model or product family and is most often based on bare board artwork. In addition there is often an assembly revision identifier to denote the generation of the artwork. If the assembly is a panel of homogeneous or heterogeneous (product-on-panel) subassemblies then it is important that the super-assembly identifier be differentiable from those of the subassemblies to prevent confusion, as in the case that the individual boards are depanelized.

3.1.4 Physical Descriptions

Besides parametric data associated with continuity and isolation, there is the category of physical data that is associating with fixturing and probing the panel/board. The first of this type of data describes the outline points of the coupon, panel or board. This is typically defined as a series of vertices which describe a closed, or close-able polygon, based on a point of origin either within

or outside of the board itself. In the case of a panel, there is the subsequent definition of the vertices of each board along with their offset and rotation relative to the panel origin. In order to maintain probe alignment, it is necessary to define the fiducial or tooling pin locations for each board relative to its own origin. Also relative to this origin are each of the pads and test-points of the board. Though each of these (X,Y) locations can be named (typically based on a device pin) or un-named, they must each maintain their association to a physical net of the board. These locations must also be allowed to carry attributes of accessibility and probable surface or direction.

4 GENERAL RULES

The following details reflect the rules in GenCAM to meet the requirements for bare board test. These rules are intended to meet the needs of the testing entity to understand the customer requirements.

Wherever necessary, additional requirements have been detailed to reflect precision. The attributes and rules for GenCAM described in IPC-2511 are referenced.

Wherever necessary, detailed descriptions or definitions of entries, attributes or characteristics are described according to the following issues detailed in table and descriptions.

Table 4-1 Bare Board Test - Keyword Usage

Need Identifier	Section Keyword	Keyword Usage
Designer, Engineer, Billing Address	ADMINISTRATION	DESIGNER.<person_ref> ENGINEER.<person_ref> BILLTO.<person_ref>
Board/Panel Identifier and Board/Panel Revision Identifier	HEADER	PANEL.<panel_number> BOARD.<board_number>
Drawings	DRAWINGS	DRAWING, DWGREF
Embedded Component Locations	COMPONENTS	COMPONENT.<place> COMPONENT.<layersingle_ref>
	LAYERS	COMPONENT.DEVICEREF.>part_ref>.VALUE
Embedded Component Values and Tolerances	DEVICES	DEVICE.VALUE.<measured_value>
Signal Names & Characteristics	ROUTES	ROUTE, IMPEDANCE, INDUCTANCE, CAPACITANCE, HIGHPOTTEST, REFERENCE
	BOARDS	BAREBOARDTEST
	PANELS	BAREPANELTEST
Physical Path & Access Attributes	ROUTES	ROUTE, PATH, PLANE, VIA, TESTPAD, COMPPIN, CONNPIN
Engineering Change Effects Corrections To Previously Sent Data	CHANGES	CHANGE, ADD, DELETE, RENAME, ADDPRODUCT, DELETEPRODUCT, RENAMEPRODUCT

Table 4-2 Bare Board Test Fixturing Keyword Usage

Need Identifier	Section Keyword	Keyword Usage
Designer, Engineer, Billing Address	ADMINISTRATION	DESIGNER.<person_ref> ENGINEER.<person_ref> BILLTO.<person_ref>
Board/Panel Identifier and Board/Panel Revision Identifier	HEADER	PANEL.<panel_number> BOARD.<board_number>
Units of Measure	HEADER	UNITS, ANGLEUNITS
Panel Footprint (Location)	FIXTURES	FIXTURE.PLACEMENT
	PANELS	PANEL.OUTLINE
Board Footprint (Location)	FIXTURES	FIXTURE. PLACEMENT
	PANELS	PANEL.PLACEMENT
	BOARDS	BOARD.OUTLINE
Board/Panel Tooling Holes and Fiducials	PANELS	PANEL.HOLEREF.<hole_type>
	BOARDS	BOARD.HOLEREF.<hole_type>
Signal Names	ROUTES	ROUTE.<net_name>
Potential Test Probing Locations, Access Attributes and Board Side	ROUTES	ROUTE.PATH, ROUTE.PLANE VIA, TESTPAD, COMPPIN, CONNPIN
	LAYERS	LAYERSINGLE, LAYERSET, LAYERSWAP
Fixture, Board/Panel Keepout Region	FIXTURES	FIXTURE.KEEPOUT
	PANELS	PANEL.KEEPOUT
	BOARDS	BOARD.KEEPOUT
Fixture Identifier	FIXTURES	FIXTURE.<fixture_ref>
Fixture Type	FIXTURES	FIXTURE.<fixture_app>
Testpoint	TESTCONNECTS	TESTCONNECT.TESTPROBE
Tester Resource Pin	TESTCONNECTS	TESTCONNECT.TESTPIN
Engineering Change Effects Corrections To Previously Sent Data	CHANGES	CHANGE, ADD, DELETE, RENAME ADDPRODUCT, DELETEPRODUCT, RENAMEPRODUCT

5 MODELING

The data files of GenCAM may be mapped to the information models. Information models are developed to ensure that complete mapping is capable between the information provided within the GenCAM characteristics. The correlation is provided in the activity models shown in IPC-2519.

All data activities are based on activity models as defined in IPC-2519. The activity models covered by CAD and CAM include the engineering, design, administrative, and fabrication and assembly characteristics. Each of these sections are intended to be detailed into various levels of activity much like layers of information needed to perform a particular manufacturing process.

Figure 5-1 shows the activity needed to develop administrative data.

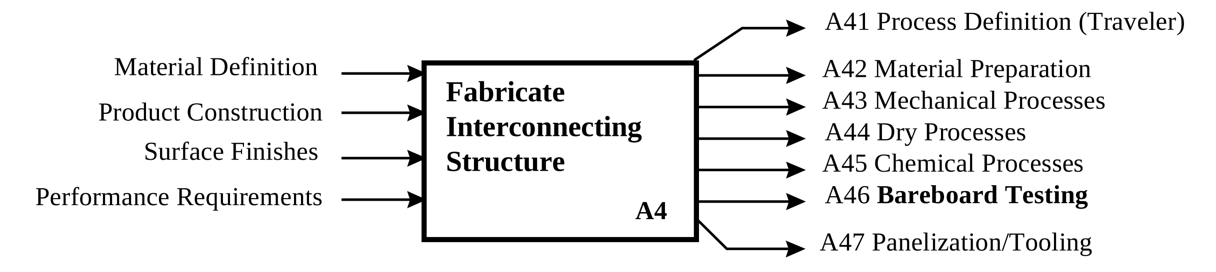


Figure 5-1 Bare board Test Activity

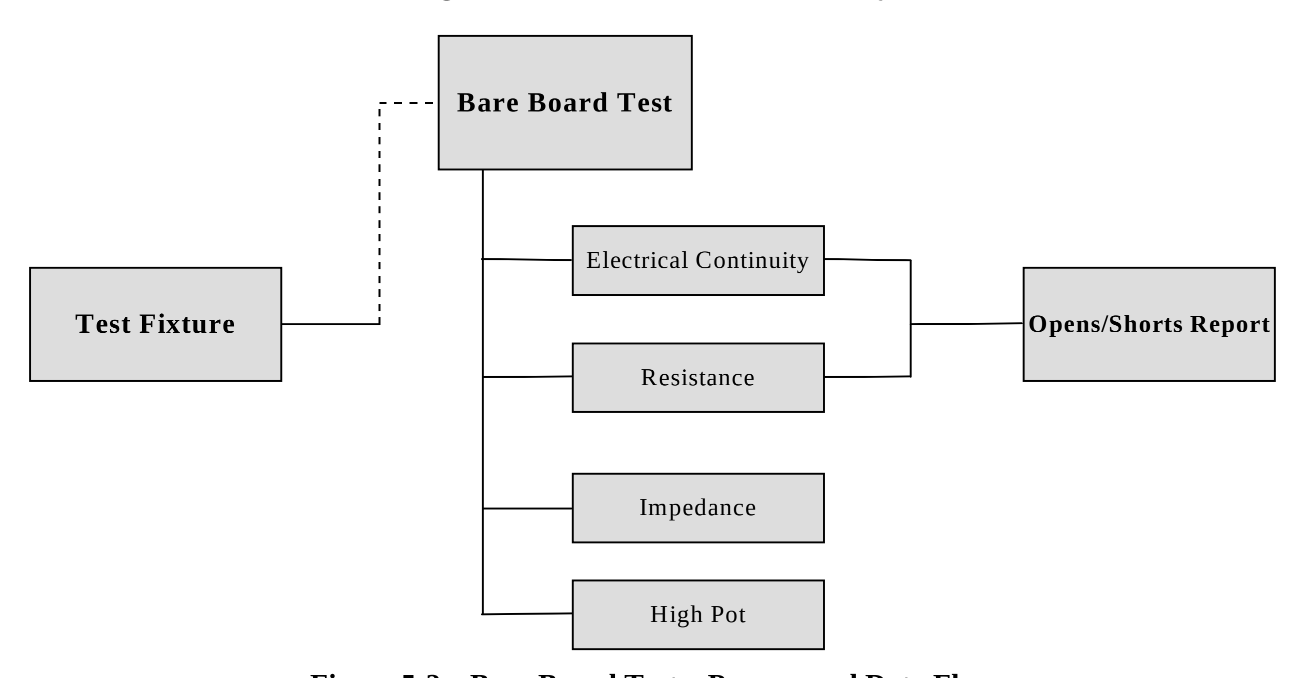


Figure 5-2 Bare Board Test – Process and Data Flow

5.1 Information Models

Information models are also helpful in understanding the requirements of the bare board product testing section. Attribute information is correlated to the parameters of GenCAM as well as to the activity models used to describe bare board electrical test data.

EXPRESS is an international information modeling format supported by ISO 10303-11. The graphic representation of EXPRESS is known as EXPRESS-G. Appendix A provides an explanation of the different EXPRESS-G requirements. Figures 5-2 through 5-5 show the EXPRESS-G version of the GenCAM FIXTURES, POWER, ROUTES and PADSTACKS sections. See www.gencam.org for complete EXPRESS-G model.

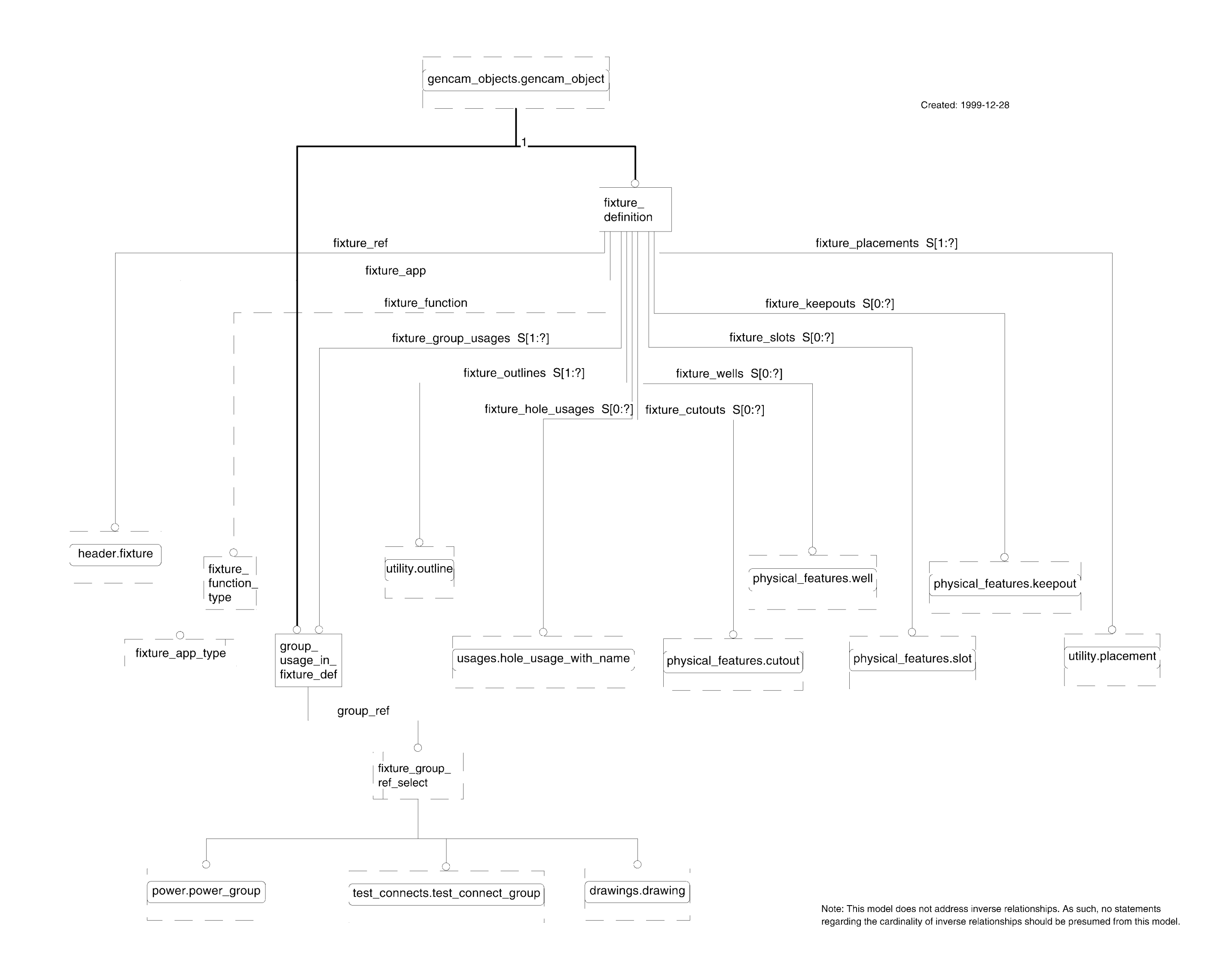
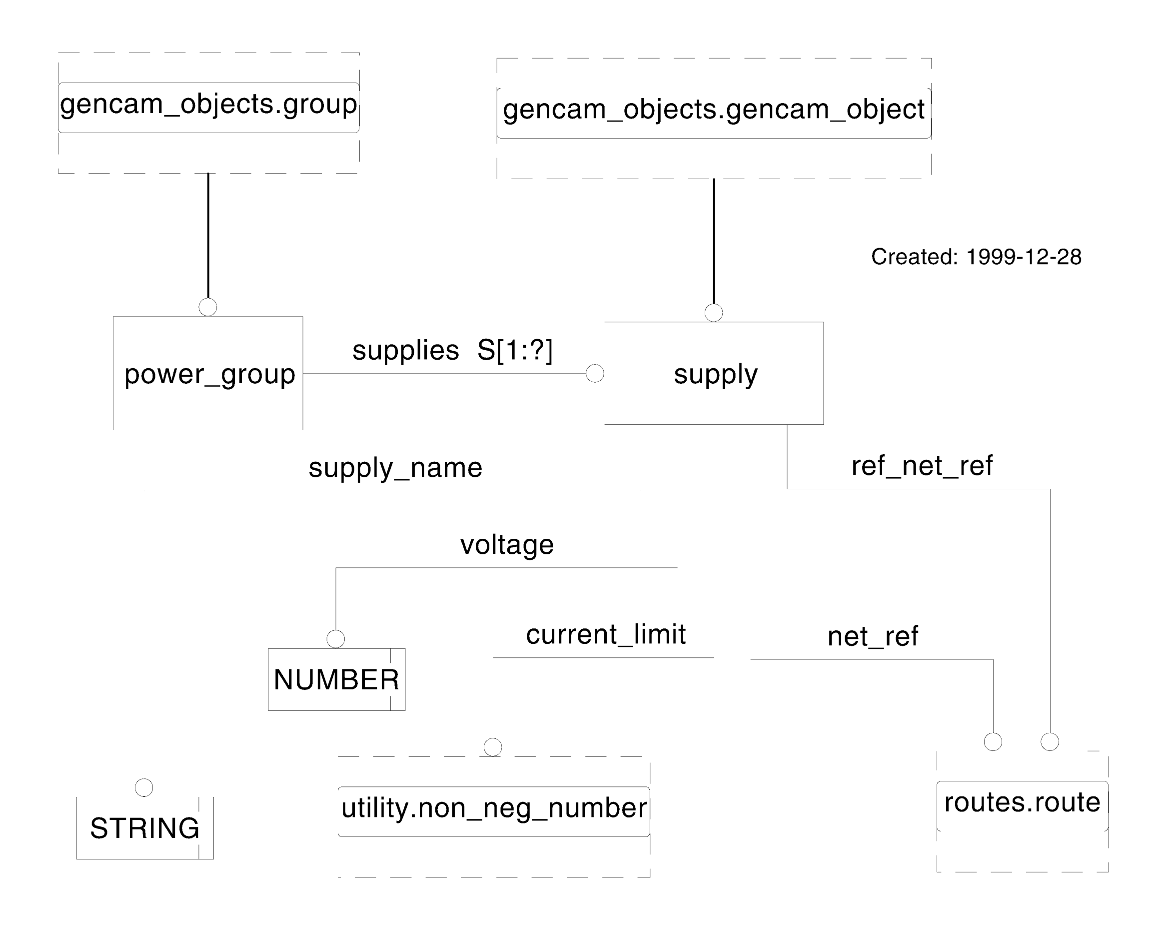


Figure 5-2 EXPRESS-G for FIXTURES



Note: This model does not address inverse relationships. As such, no statements regarding the cardinality of inverse relationships should be presumed from this model.

Figure 5-3 EXPRESS-G for POWER

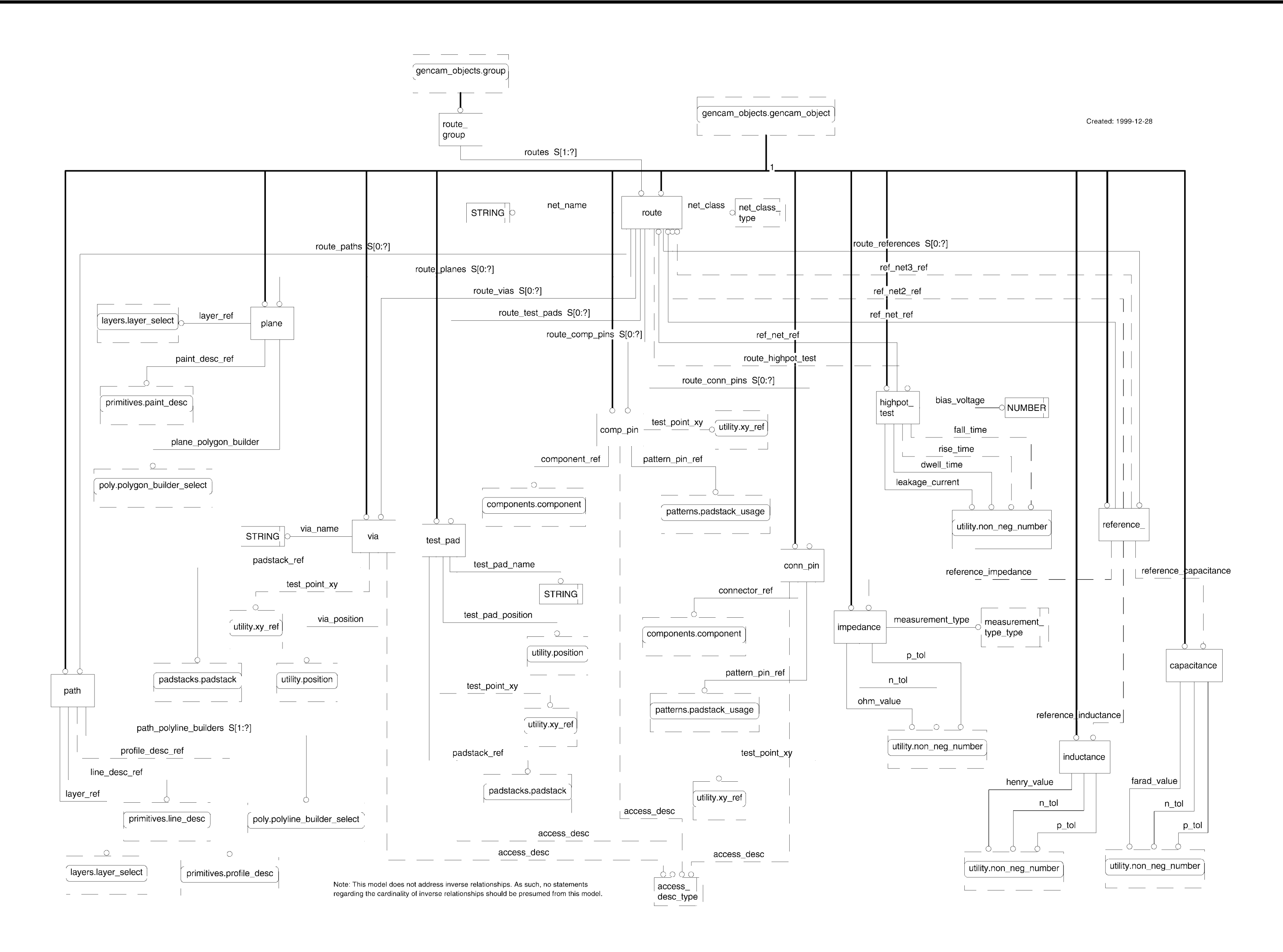


Figure 5-4 EXPRESS-G for ROUTES

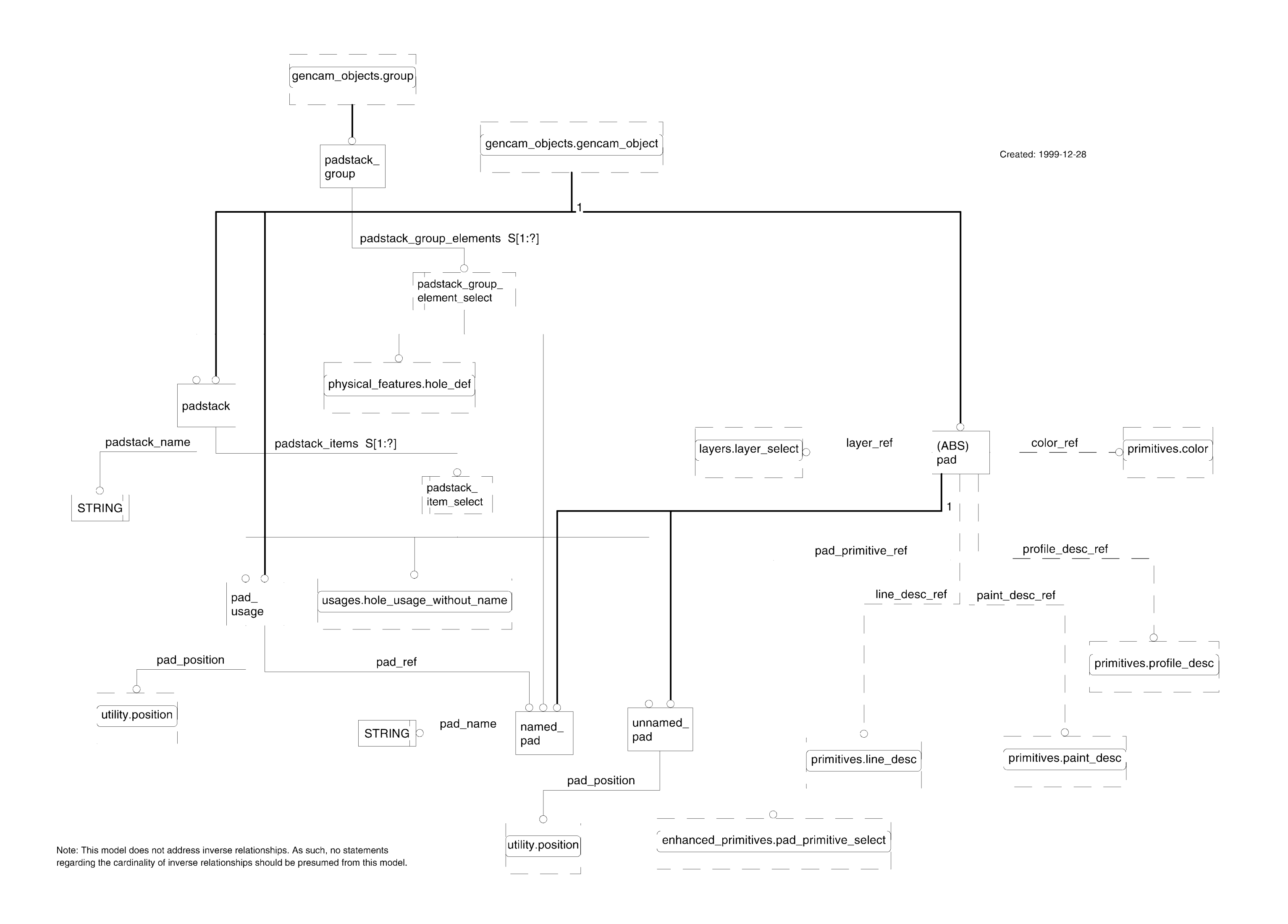


Figure 5-5 EXPRESS-G for PADSTACKS

6 REPORT GENERATORS

Data can be extracted from GenCAM files to produce various formats that are commonly used in the electronics industry. The types of reformatting can be used for electronic data transfer to tools or to facilitate inspection and human interpretation of text and/or graphic rendering. Note that no extraction tools are included in the IPC-2510 standard. Their creation is left to the industry as the need arises.

Figure 6-1 shows examples of bare board test requirements.

An example of an IPC-D-356 test file is shown below with an explanation of the format. The format is a fixed 80 character format with data having significance in the column position.

Column 1 3 = Point record
Column 2 1 = Feature and through-hole at point location
Column 3 7 = Standard electrical TEST data
Column 4-17 = Net identifier
Column 21-26 = Component Identifier
Column 27 = Dash separator between component identifier and pin number
Column 28-31 = Pin identifier
Column 33-37 = D in column 33 is diameter and 34-37 is the hole diameter in 0.0001"
Column 38 = P is PTH hole, U is non-PTH
Column 39-41 = A in 39 is access, 00 in 40-41 is two sided access
Column 42-57 = X-Y location
Column 58-62 = X feature dimension
Column 63-67 = Y feature dimension
Column 73-74 = Soldermask field where S0 is no soldermask on both sides

A sample file of IPC-D-356 follows:

```
C  File generated by Bare Board TestGen, V3.4
C  Board Number:    5022604 01 A1
C  Generation Date: December 15, 1993, 12:15 A.M.
C
P  JOB   SINGLE BREAKOUT BOARD IPC356 TEST DATA
P  FORM F(ixed)
P  CODE 01
P  UNITS CUST
P  TITLE SINGLE BREAKOUT BOARD
P  NUM   50-22604-01
P  REV   A1
P  LANG  SDEF    03
C  Bare board test data
C  This data conforms to IPC-D-356, Initial Release "-", March 1992
P  VER "-"
P  DIM n
1234567890123456789012345678901234567890123456789012345678901234567890112345
317VCC                  P2    -96   D 380PA00X  30300Y  21600 X 550 Y 550        S0
3172                    P2    -95   D 380PA00X  31300Y  21600 X 550 Y 550        S0
```

```
317GND               P2    -94   D 380PA00X  32300Y  21600 X 550 Y 550        S0
3171                 P2    -86   D 380PA00X  40300Y  21600 X 550 Y 550        S0
317146               P2    -93   D 380PA00X  33300Y  21600 X 550 Y 550        S0
317145               P2    -92   D 380PA00X  34300Y  21600 X 550 Y 550        S0
317144               P2    -91   D 380PA00X  35300Y  21600 X 550 Y 550        S0
317143               P2    -90   D 380PA00X  36300Y  21600 X 550 Y 550        S0
317142               P2    -89   D 380PA00X  37300Y  21600 X 550 Y 550        S0
317141               P2    -88   D 380PA00X  38300Y  21600 X 550 Y 550        S0
317140               P2    -87   D 380PA00X  39300Y  21600 X 550 Y 550        S0
C
C  Total Number of Test Points: 11
C
C  Number of Side 1 Surface Mounted Component Pads: 0
C  Number of Side 2 Surface Mounted Component Pads: 0
C  Number of Component Pin Holes:              11
C  Number of Finger Pads:                            0
C  Number of Test Pads:                              0
C  Number of Vias:                                   0
C  Number of Tooling Holes:                    3
C
C       NETWORK NAME TABLE
C
C
C  NNAME1    GND
C  NNAME2    VCC
C  NNAME146
C  NNAME145
C  NNAME144
C  NNAME143
C  NNAME142
C  NNAME141
C  NNAME140
999
```

Figure 6.1 IPC 356 Bare Board Test File

7 REFERENCE INFORMATION

The following sections define reference documents that are useful in clarifying the products or process of the industry or provide additional insight into the subject of data modeling or released information models.

7.1 IPC (1)

IPC-2221	Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies
IPC-D-300	Printed Board Dimensions and Tolerances
IPC-D-310	Guidelines for Artwork Generation and Measurement Techniques for Printed Circuits
IPC-D-325	Documentation Requirements for Printed Boards, Assemblies and Support Drawings

7.2 American National Standards Institute (2)

ANSI X3/TR-1-77	American National Dictionary for Information Processing
ANSI X3.12	Subroutine Record Format Standardization
ANSI Y14.5	Dimensioning and Tolerancing for Engineering Drawing
ANSI Y32.1	Logic Diagram Standards
ANSI Y32.16	Electrical and Electrical Reference Designators
ANSI Z210.1	Metric Practice Guide (ASTM 380-72)

7.3 Department of Defense (3)

DoD-STD-100	Engineering Drawings

7.4 Electronic Industries Association (4)

EDIF 4 0 0	Electronic Data Interchange Format

7.5 International Organization for Standards (ISO)

ISO STEP Documentation

AP210	Electronic Printed Circuit Assembly: Drawings and Manufacturing
AP211	Electronic PC Assembly, Test Diagnostics & Remanufacture
AP221	Process Plant Functional Data & Schematic Representation

Appendix A

EXPRESS defines data objects and their relationships among data objects for a domain of interests. Some typical applications of data models include supporting the development of databases and enabling the exchange of data for a particular area of interest. As an example, a specific requirement of a database for an audio compact disc (CD) collection is shown in Figure 1.

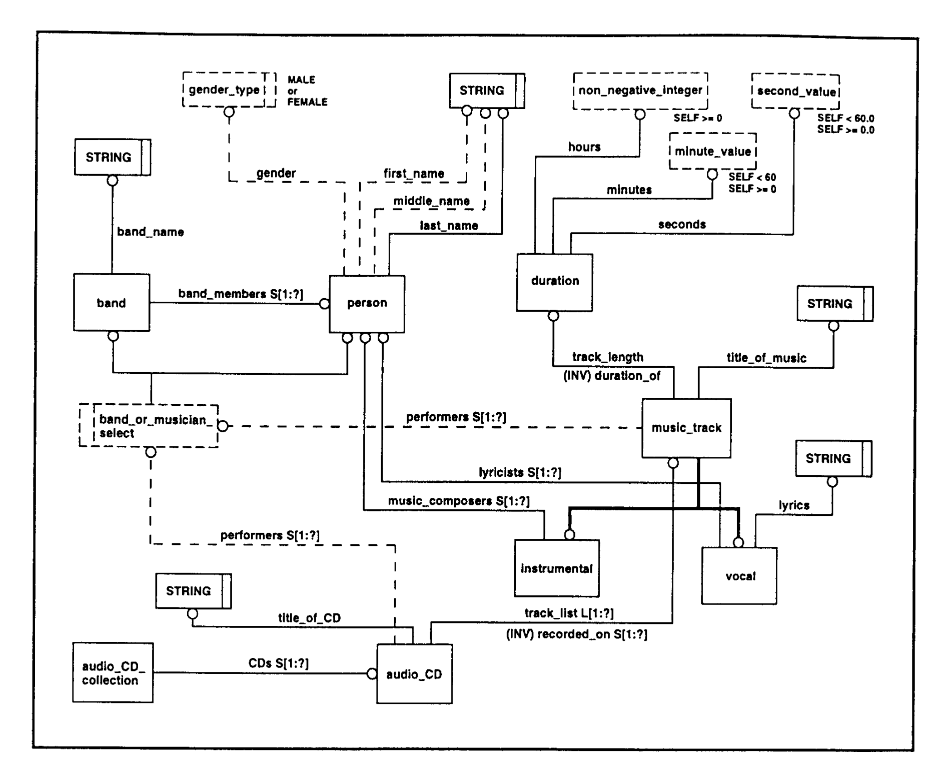


Figure A-1 Example of EXPRESS-G Model

Data models are specified in a data modeling language. EXPRESS is a data modeling language defined in ISO 10303-11. One of the advantages of using EXPRESS-G over EXPRESS is that the structure of a data model can be more intuitively presented. A disadvantage of EXPRESS-G is that complex constraints cannot be formally specified. There are specific symbols used in EXPRESS-G notation. The meaning of those symbols is defined in the EXPRESS formatting.